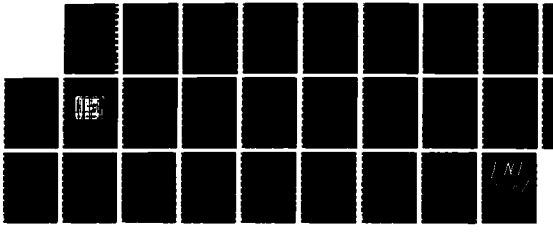
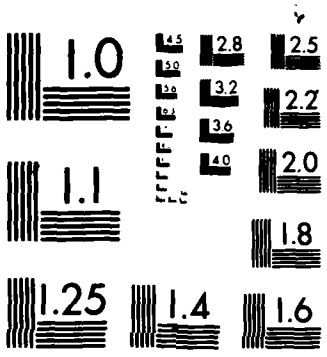
AD-A176 094 SEU (SINGLE EVENT UPSET) VULNERABILITY OF THE ZILOG Z-80 AND NSC-800 MICR (U) AEROSPACE CORP EL SEGUNDO CA R KOGA ET AL 30 SEP 86 TR-0086(6940-05)-18 SD-TR-86-70 1/1

UNCLASSIFIED F04701-85-C-0086 F/G 9/2 NL





REPORT SD-TR-86-70

SEU Vulnerability of the Zilog Z-80 and NSC-800 Microprocessors

R. KOGA, W. A. KOLASINSKI, and C. KING
Space Sciences Laboratory
Laboratory Operations
The Aerospace Corporation
El Segundo, CA 90245
and
J. CUSICK
Analex Corporation
Cleveland, OH 44135

30 September 1986

Prepared for
SPACE DIVISION
AIR FORCE SYSTEMS COMMAND
Los Angeles Air Force Station
P.O. Box 92960, Worldway Postal Center
Los Angeles, CA 90009-2960

This report was submitted by The Aerospace Corporation, El Segundo, CA 90245, under Contract No. F04701-85-C-0086 with the Space Division, P.O. Box 92960, Worldway Postal Center, Los Angeles, CA 90009-2960. It was reviewed and approved for The Aerospace Corporation by H. R. Rugge, Director, Space Sciences Laboratory. Capt Douglas R. Case, SD/YCM, was the project officer for the Mission Oriented Investigation and Experimentation (MOIE) program.

This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

Douglas R. Case

DOUGLAS R. CASE, Capt, USAF
MOIE Project Officer
SD/YCM

Joseph Hess

JOSEPH HESS, GM-15
Director, AFSTC West Coast Office
AFSTC/WCO OL-AB

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER SD-TR-86-70	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* SEU VULNERABILITY OF THE ZILOG Z-80 AND NSC-800 MICROPROCESSORS		5. TYPE OF REPORT & PERIOD COVERED 6. PERFORMING ORG. REPORT NUMBER TR-0086(6940-05)-18
7. AUTHOR(s) R. Koga, W. A. Kolasinski, C. King, and J. Cusick		8. CONTRACT OR GRANT NUMBER(s) F04701-85-C-0086
9. PERFORMING ORGANIZATION NAME AND ADDRESS The Aerospace Corporation El Segundo, CA 90245		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Space Division Los Angeles Air Force Station Los Angeles, Calif. 90009-2960		12. REPORT DATE 30 September 1986 13. NUMBER OF PAGES 29
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Microprocessor
NSC-800
Single-Event Upset
Z-80

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

A detailed analysis of the SEU vulnerability of the Zilog Z-80 microprocessor is presented based upon data obtained with heavy ions and protons. The analysis demonstrates a method for separating upsets of the general purpose registers from upsets of the internal latches. Furthermore, the analysis shows that the bulk of the upsets observed below a LET value of 4 MeV-cm^2/mg is associated with upset of these internal latches. To obtain

DD FORM (FACSIMILE) 1473

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

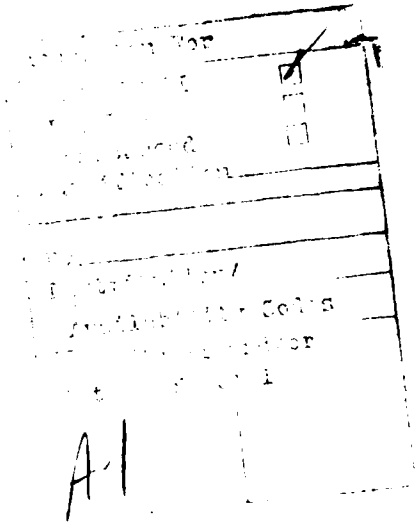
19. KEY WORDS *(Continued)*

20. ABSTRACT *(Continued)*

the data which made this analysis possible, a novel test technique was developed which associates all upsets with the machine cycle during which they first appear on the device pins. Limited data for the NSC-800 are included.

PREFACE

The authors acknowledge the helpful discussions of the Z-80 architecture with Lawrence E. Larsen, James D. Meddleton, and Richard Workover of Zilog Corporation. We also acknowledge the many helpful discussions on device physics and data analysis with Dr. Donald R. Behrendt of NASA Lewis Research Center.



CONTENTS

FIGURES

TABLES

I. INTRODUCTION

The single event upset (SEU) hazard of a microprocessor (μP) may not be recognized until late in the development cycle of the spacecraft system. At that time, replacement of one μP with another, using a different instruction set, is not a realistic solution due to the extensive software development effort already invested as well as the impact of such an action upon cost and schedule. Other alternatives do exist which may involve hardware changes but will allow the system to tolerate certain types of SEU errors and recover successfully from the rest.

Many SEU errors will affect data or computed results in a fashion similar to the errors arising from other electrical and EMI noise sources. Immunity from these SEU errors is already provided by noise immunity techniques. Other kinds of SEU errors in the μP are capable of causing system malfunctions that were never considered possible when the system requirements were defined. The first task in developing a survival strategy for this type of error is to identify the storage nodes that may cause these catastrophic system failures and to define the SEU cross section for upset of those nodes.

Published results[1] show the consequences of some μP upsets, and suggest that the program counter (PC) and stack pointer (SP) are two critical nodes. Upset of these registers can cause a program jump that writes over portions of memory before ending up in an idle loop or coming to a complete halt. In addition to the general purpose register (GPR) upsets, other internal nodes can be upset, and some of these upsets may have similar adverse effects on system operations.

This work was motivated by the need to define the SEU vulnerability of the Zilog Z-80, an NMOS μP, which is to be used aboard the Space Shuttle to control the Centaur upper stage from lift-off until Centaur separation. The cosmic ray environment for the baseline Shuttle orbits with inclination angles less than 45° present no real SEU hazard.[2-5] At higher inclinations, the geomagnetic shield becomes more transparent and the risk of upset can be significant. The NSC-800 was also tested. This CMOS device uses the Z-80

instruction set and was considered to be a candidate for retrofit if the Z-80 proved too vulnerable.

Many previous studies of μPs[6-10] used a reference device or "golden chip" (GC) to recognize the occurrence of an upset error. For the heavy ion tests, a "device" cross section was usually determined, however, the results were often influenced by the choice of test software routines and represented an average response of device and software. For our needs, a more specific test of the device is required to define the upset cross section of the major μP subsystems such as the GPR, internal latches, and control lines.

The objectives of these experiments are to: (1) develop a μP test method that can provide device-error data in sufficient detail to permit separation of the GPR upsets from the internal latch upsets, (2) determine the cross section and LET threshold for the GPRs, (3) determine the upset contribution of the internal latches, and (4) examine the bit errors that reach the control lines to find error patterns that may pose unexpected hazards to system operations.

II. EXPERIMENTAL

Heavy ion testing was performed at the Berkeley 88" Cyclotron and at the ORNL Tandem Facility. Proton testing was performed at the University of Indiana Cyclotron. The charged particle beam-control and exposure apparatus that was used in the heavy ion tests is described in detail elsewhere.[11] Heavy ion bombardment is performed in vacuum with device lids removed. Proton tests employed an abbreviated version of the beam exposure apparatus described above, and the tests were performed in air. Three Z-80 and three NSC-800 devices were used in these tests.

The heavy ion particle beams used in these tests span the linear energy transfer (LET) scale from 0.7 to 17.7 MeV-cm^2/mg. A list of the ion, energy, and LET is given in Table 1. Proton energies of 100 and 200 MeV were used for the Z-80 tests. No proton tests were performed on the NSC-800.

1. DATA ACQUISITION

The Intelligent Memory Controlled Operation (IMCO)* test method we use employs a golden chip for error recognition, but uses a gated hardware comparator to test all device output pins for error at the end of each machine cycle. This approach will identify errors at the sub-instruction level at their first appearance on the device pins. When an error is detected, all 32 output pins (16 address, 8 data and 8 control) of both the device under test (DUT) and the GC are recorded in a diskette error file.

A DEC LSI/11-23 computer is the controller used in the IMCO method. It controls all test sequences and acts as memory and I/O device for both the DUT and GC. Both chips receive program instructions in parallel from the IMCO. The IMCO also decodes the Z-80 opcodes so that it can issue "wait" instructions to the Z-80s to allow more time for error checking and other housekeeping tasks.

*The Intelligent Memory Controlled Operation test method was developed by C. King.

Table 1. Ion Species, Energies, and Linear Energy Transfer (LET) for Ion Beams Used in These Tests.

Ion Species	Energy (MeV)	LET ($MeV\text{-}cm^2/mg$)
Argon	84	17.73
	176	14.28
Neon	92	5.46
Oxygen	37	5.12
	150	2.23
Nitrogen	69	2.75
Carbon	121	1.22
	240	0.73
Hydrogen	100	0.005
	200	0.0036

As a result, the Z-80 instruction rate is reduced to a few hundred instructions per second. Both devices are synchronized by a 1-MHz clock line.

2. GENERAL PURPOSE REGISTERS

The general purpose register-memory cell of the Z-80 is a six transistor design using depletion mode load transistors. An electron photomicrograph of a general purpose register cell from a device used in these tests is shown in Fig. 1. From this figure the maximum area of the Z-80 GPR memory cell is 3141 μm^2 (3.141 x 10E-5 cm^2). Since each memory cell contains two bits, the maximum area of a single bit is taken to be 1570 μm^2 (1.57 x 10E-5 cm^2).

3. INTERNAL LATCHES

In the Z-80, the 32 output signals are connected to the device pins by means of dynamic latches which are refreshed on each rising clock cycle (T-state). These bus latches form a subset of the internal latches and contribute directly to any upsets seen on the device pins. Other internal latches are used to load, move, and manipulate data in the GPRs. Upset of these latches will also contribute to the errors seen on the device pins. The size of this contribution will be instruction dependent.

Upset errors for a group of internal latches can be seen by studying the errors in the control lines. The control signals are generated during instruction decoding and are stored internally until being placed on the control lines when the proper machine cycle is executed. Control-line bits are not directly accessible to the programmer and do not communicate with the GPRs. Thus, control-line errors must arise exclusively from the upset of internal storage nodes other than the general purpose registers.

4. TEST SOFTWARE

The software routines used in these tests were designed to display upsets in the general purpose registers. A family of software test routines were used individually and concatenated into larger routines to survey the upset sensitivity of the Z-80 to different program instructions.

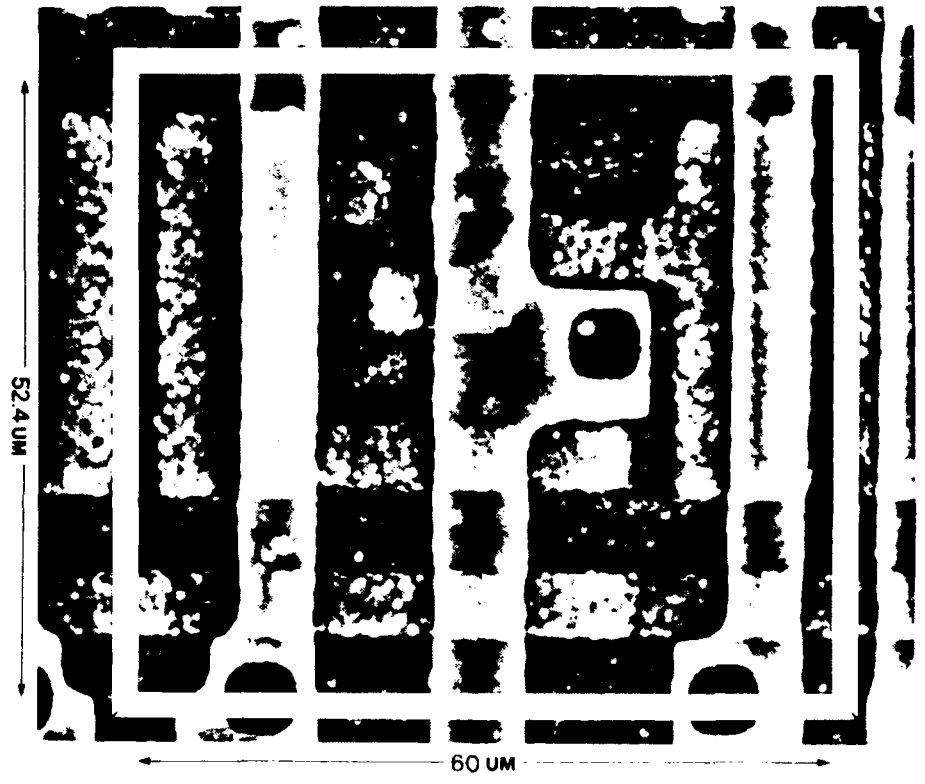


Fig. 1. Photomicrograph of the Z-80 General Purpose Register Memory Cell Used in This Study. The area of the cell is 3141 μm^2 (3.141 × 10E-5 cm^2). Each cell contains two bits. Thus, the cell area for one bit is 1570 μm^2 (1.57 × 10E-5 cm^2)

Program 66 is the most useful in revealing upsets in the GPRs. This routine effectively tests all 26 GPRs by checking each register sequentially, in a continuous loop, until an error is detected. This routine uses the "push" instruction exclusively to output each of the 22 8-bit registers and minimizes internal latch upsets by limiting register manipulation.

The other test routines test less than 26 8-bit registers due to the instructions used to survey the various Z-80 operations. For these routines, the object code was analyzed to derive an average number of registers tested. That value is used to normalize the computed cross section and appears in the legend of the appropriate data figure. These routines perform more register manipulations and therefore allow more internal latch upsets in the data.

III. RESULTS AND DISCUSSION

A. Z-80 TESTING

An overall summary of the Z-80 upset errors is given in Table 2. The bit map shown lists the frequency and location of errors by bit-flip count. The single bit errors in the address and data lines are used to display the upset cross section of the general purpose registers. Errors having multiple bit-flips suggest more complicated pathways to the device pins from the site of the initial upset. The probability of two or more upsets within the time needed to complete a software loop is very small.

The heavy ion data for the Z-80 are shown in Fig. 2. Data from each test routine are normalized by the average number of 8-bit registers tested. The value used is given in the legend. The maximum area of a single GPR bit is also indicated.

There are several features of this data that will be addressed by our analysis. First, the gradual slope of the data over most of the measured range of LET does not reveal a LET threshold for the GPR. The slope is more gradual than is usually seen in RAM tests.[11] Second, considerable scatter is seen in the measured data that is not a consequence of the register normalization process. And finally, the cross section at high LET does not show much tendency towards saturation, and the measured values exceed the maximum area of a single general purpose register bit.

The data of Fig. 2 represent "device" cross section data of the type normally obtained in heavy ion tests. Each data point includes all the errors from all nodes in the device that are upset. Our analysis makes use of the detailed error data recorded with each observed error and selects those errors that occur on certain device pins during certain machine cycles.

1. GENERAL PURPOSE REGISTERS

The first machine cycle of every program instruction is called the "opcode fetch" cycle. At the end of this machine cycle the PC is on the address line. Computing the cross section for single bit errors in the

Table 2. Z-80 Bit Error Frequency Map - Overall Summary

Number of Bit Flips, Observed Frequency, and Line Location

Bits	Address	Data	<A+D>	Control	<A+C>	<D+C>	<A+D+C>
>9	153	0	7	0	0	0	0
=9	70	0	2	0	0	0	0
=8	123	32	0	0	3	0	9
=7	141	11	3	0	7	0	75
=6	130	48	3	0	86	0	209
=5	100	79	4	0	192	3	184
=4	131	177	5	0	246	8	77
=3	144	131	5	17	104	56	13
=2	251	189	6	47	40	3	0
=1	4737	3067	32	647	45	0	0
Totals =	5980	3734	67	711	723	70	567 = 11852

587 Illegal control line values are observed:

301 Errors have both "read" and "write" lines active

245 Errors have memory and I/O control interchanged

41 Errors have the "halt" line active

NOTE: Errors having bit-flips in Address and Data lines are listed in column <A+D>. The total number of bit-flips divided by 2 defines the "Bit" row for the entry. C denotes control lines. In column <A+D+C> the total bit-flip count is divided by 3. (Integer division).

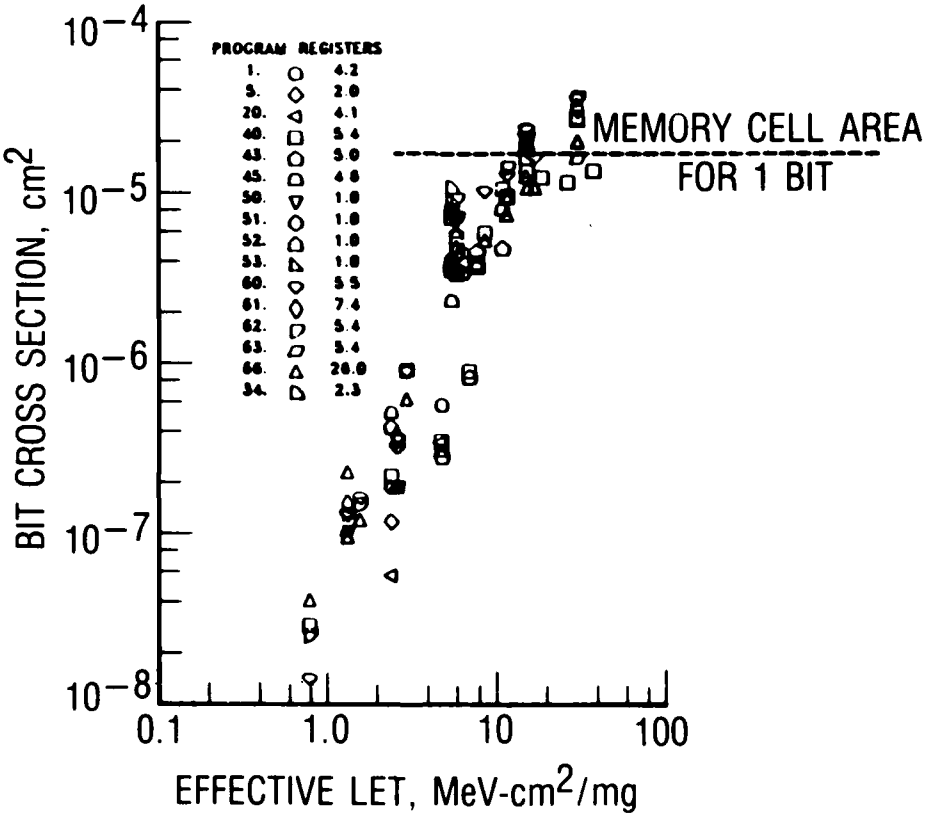


Fig. 2. Total Device Upset Cross Section for the Z-80. Heavy ion data using 16 different test software routines. The number of 8-bit registers tested in a given routine is indicated in the legend. Cross section is on a "per bit" basis. Also shown is the area for a single register bit.

address lines during the opcode fetch machine cycle gives the results shown in Fig. 3. Each data point shown is a mixture of PC upsets and internal latch upsets.

The plot shows evidence of an LET threshold near 4 MeV-cm^2/mg. There are 18 additional data points with LET <4.0 MeV-cm^2/mg that do not appear on the figure because their cross section values are less than 1 μm^2 (1.0 × 10E-8 cm^2). All data points having cross sections less than 50 μm^2 (5.0 × 10E-7) represent areas that are too small to be features of the PC. These data points must represent a larger feature, but one with a small duty cycle for upset. The internal latch would display this property.[12]

A similar analysis can display the cross section for upset of the stack-pointer (SP). Program 66 uses the "push" instruction exclusively for memory-write operations. Consequently, each memory-write machine cycle for program 66 will have the SP on the address lines and one of the 22 8-bit GPRs on the data lines. Using data from program 66 and computing the cross section for single bit address-line errors at the end of the memory-write machine cycle gives the results shown in Fig. 4.

The cross section of the remaining 22 8-bit general purpose registers can be displayed all at once by plotting the cross section for single bit errors in the data lines during the memory-write cycle of program 66. The result is given in Fig. 5.

These three figures present evidence for a LET threshold at about 4 MeV-cm^2/mg for all 26 general purpose registers. In each figure, however, the measured cross section at higher LET values exceeds the single bit area for the general purpose register (1570 μm). This observation can only mean that other upset sites, such as the internal latches, are contributing to the measured error data in this region. We expect the GPR registers to exhibit a cross-section saturation at LET values slightly above the upset threshold like that seen in RAM tests.[11] The rising slope of the measured data in the GPR saturation region (see Figs. 2 through 5) supports the inference that the internal latch error contribution continues to increase throughout this LET range.

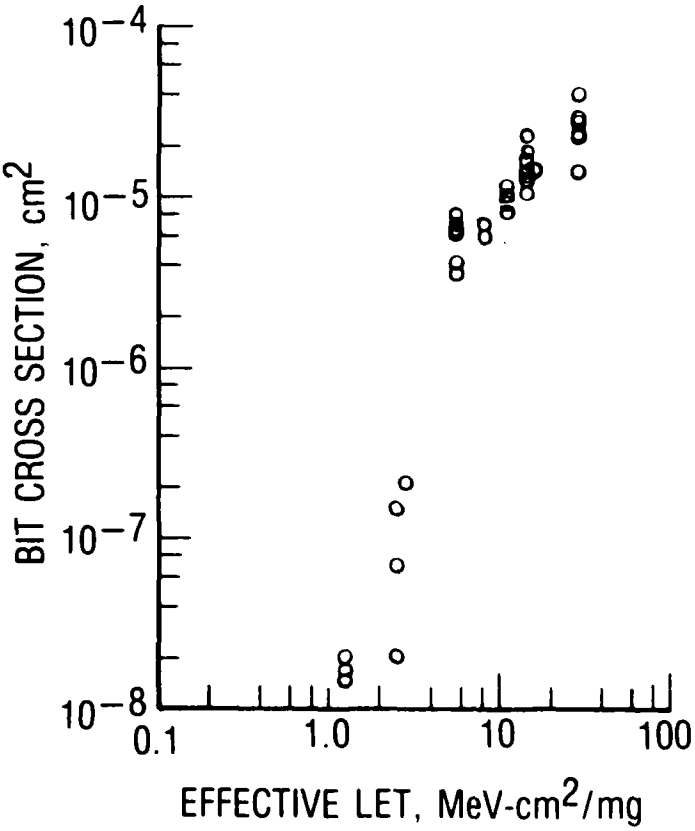


Fig. 3. Upset Cross Section for a Single Bit Address Line Error During the Opcode Fetch Machine Cycle of the Z-80. Plot shows program counter upsets (see text).

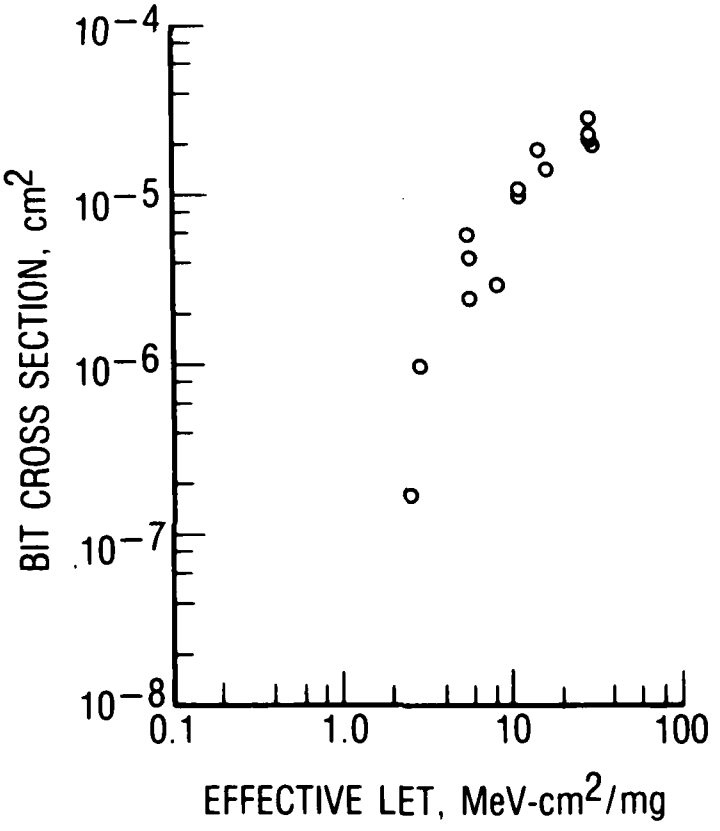


Fig. 4. Upset Cross Section for a Single Bit Address Line Error During the Memory-Write Cycle of Program 66. Plot shows stack pointer upsets (see text).

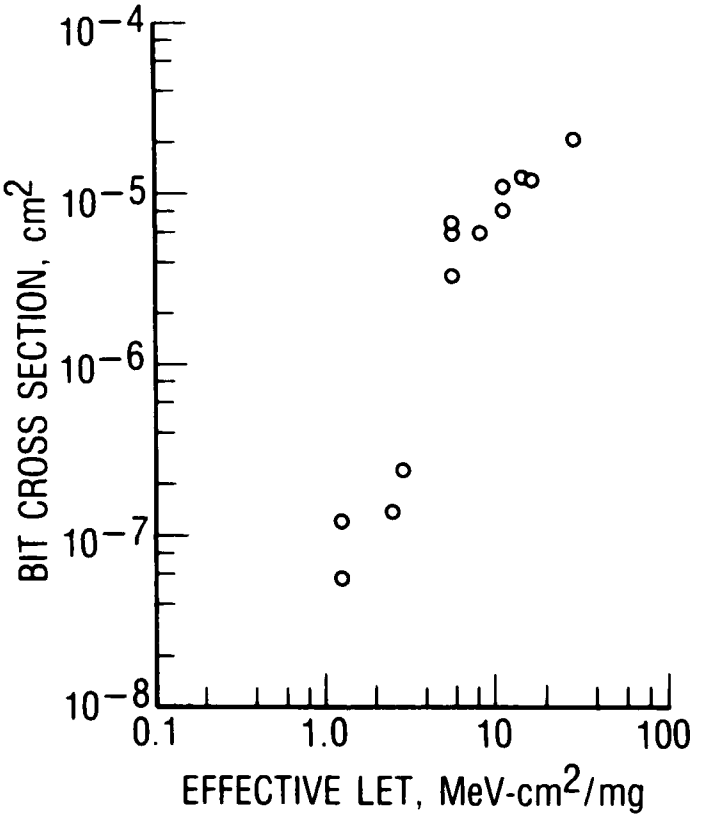


Fig. 5. Upset Cross Section for a Single Bit Data Line Error During the Memory-Write Cycle of Program 66. The plot shows the remaining 22 8-bit register upsets.

2. INTERNAL LATCHES

The upset cross section for a group of internal latches can be computed using single bit errors in the control-lines during the opcode fetch machine cycle. Since this cycle is common to all test programs, data from all test programs can be used to get a more complete result. Figure 6 presents a plot of this data.

In general, different machine cycles are expected to use different groups of internal latches in different ways. Consequently, we would expect the cross section for upset in the control lines to differ from one kind of machine cycle to another. The error data show that out of the 3465 errors seen during the opcode fetch cycle, 447 errors were in the control-lines. This is the largest percentage of control-line errors among the different machine cycles. The smallest percentage of control errors occurred during the memory-write cycle. In that case, only 76 control-line errors occurred out of a total of 5763 errors. The cross section for a single bit control-line error during the memory-write cycle is about one-fifth as large as the cross section for a single bit control-line error in the opcode fetch cycle shown in Fig. 6.

The scatter seen in the internal latch cross section data explains the origin of the scatter observed in the cross section data of Figs. 2 through 5. The magnitude of the internal latch cross section increases in the same gradual manner as the data in Fig. 2 both below and above the LET threshold for the GPR. In the higher LET region the internal latch cross section increase is similar to the increase seen in Figs. 3 through 5. Eventually, the data show that the cross section exceeds the area of the GPR stored bit, namely, 1570 μm. An accurate measurement of the saturation cross section for the GPR is impossible from data with such large variability, however, an estimated value of $1.5 \times 10E\text{-}5$ cm^2 appears reasonable.

The internal latch (IL) cross section for all machine cycles is reasonably well bounded by the two expressions:

$$\text{IL Cross Section} = 2.0\ E\text{-}7 \times LET^{1.9}\ cm^2 \quad LET < 5.0\ MeV\text{-}cm^2/mg$$

$$\text{IL Cross Section} = 1.0\ E\text{-}6 \times LET^{1.0}\ cm^2 \quad LET < 5.0\ MeV\text{-}cm^2/mg$$

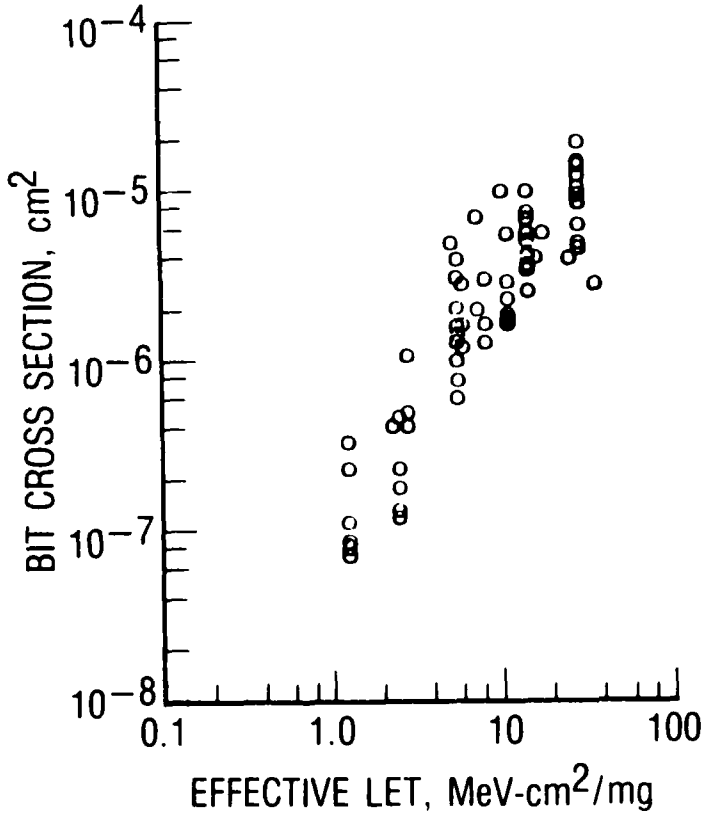


Fig. 6. Upset Cross Section for a Single Bit Error in the Control Lines During the Opcode Fetch Cycle. Data from all test programs are used. Plot displays the internal latch upsets associated with the opcode fetch machine cycle. Each machine cycle has a cross section similar to this figure.

These expressions imply the existence of two distinct types of internal latch. The "slow" latch dominates the data above 5 MeV-cm^2/mg with a linear LET dependence, and the "fast" latch is seen at lower LET and varies with the 1.9 power of LET. The change in exponent implies that the "fast" latches reach saturation near 5 MeV-cm^2/mg. This may be an artifact of the curve fit since a closer look at Fig. 6 could support the hypothesis that both latch types have about the same exponent but a discontinuity occurs near 5 MeV-cm^2/mg. Either case leads to the conclusion that the "slow" latch has a LET threshold near 5 MeV-cm^2/mg.

Comparing the register data of Figs. 3 to 5 with the "device" data of Fig. 2 and the "internal latch" data of Fig. 6 shows that the "fast" latch errors are greatly reduced in the register data, whereas the "slow" latch errors are about the same. This comparison shows that the distinction made between "fast" and "slow" latches is real.

The "fast" latches are thought to be internal latches primarily used for manipulation, decoding, computation, and signal transmission inside the μP. These latches are designed for high speed at low power and have small circuit loading. A small nodal charge is expected in these latches. Discussions with Zilog suggest that electrical interference between these high speed latches and other circuit elements led to hand routing for many of these nodes. Since each node is tailored to its particular circuit requirements, there is a distribution of nodal charge for these latches. Hand routing will result in larger node areas so the small capacitance must be obtained by using greater depletion depth. All these items contribute to the low LET sensitivity for the "fast" latches.

The "slow" latches are thought to be slower speed, higher power latches designed to handle large and variable circuit loads. A larger nodal charge is expected for these nodes and a larger LET threshold for upset. The bus latches seem to be good examples of the "slow" latch.

The large scatter in the internal latch data could result from several sources. The dynamic character of these latches makes the number of errors vary with the latch contents. The voltage "droop" of dynamic latches makes

the latch more sensitive just prior to refresh. Refresh time varies with instruction mix and clock frequency. "Droop" varies with refresh time and circuit loading of the node.

There is a purely statistical scatter in the data since the number of errors entering the cross-section calculation in some cases is small. A factor of 2 should account for this variance in most cases but the observed scatter in the data is more like a factor of 10. The close design margins for many "fast" latches could allow process variations to contribute to the scatter in this data. Data in this study are not adequate to determine the source of the observed scatter.

3. PROTON TESTS

Proton testing of the Z-80 with 100 and 200 MeV protons at normal incidence led to the results of Table 3. These data show that the Z-80 is not upset by protons directly,[13-16] however nuclear recoil upsets are observed at very large fluences. The energies used should reveal any proton sensitivity of the Z-80.[17]

B. NSC-800 TESTING

A limited number of heavy ion tests were performed on the NSC-800. In all, 30 data runs were made using argon and neon ions. Of these runs six were terminated when latchup or abnormal error rates were observed. Six other runs went to completion without any errors being recorded. Detailed error data were recorded on 22 runs. Those data are summarized in Table 4. The soft error data from the six latchup runs are included in Table 4 but the "non-random" and latchup errors are removed.

A plot of the soft error cross section data for the NSC-800 is shown in Fig. 7. Also shown is our best estimate for the latchup cross section in which the first occurrence of the non-random error is treated as though it were a latchup event.

Comparing the soft upset data of Fig. 7 with the Z-80 data of Figs. 2 through 6 suggests to us that the NSC-800 soft errors may be upsets in the internal latches of the NSC-800 rather than upsets in the GPRs. Whereas the

Table 3. Proton Testing Summary for the Z-80

100 MeV Protons at Normal Incidence			200 MeV Protons at Normal Incidence		
Run Number	Protons/cm^2 $x10^6$	Errors	Run Number	Protons/cm^2 $x10^6$	Errors
18	5.61	0	49	158.	0
19	83.3	0	50	5610.	5
20	72.2	0	52	772.	0
21	55.7	0	53	5550.	3
22	57.2	0	54	5550.	0
23	55.7	0	55	5550.	2
24	56.1	0			
25	5.72	0			
26	2.39	0			
27	3430.	5			
28	5890.	1			

Table 4. NSC-800 Bit Error Frequency Map

Number of Bit-Flips, Frequency Observed and Line Location (Latchup Errors Removed)			
Bits	Address	Data	Control
>9	2	0	0
=9	1	0	0
=8	0	1	0
=7	4	1	0
=6	0	0	0
=5	3	0	0
=4	3	2	0
=3	4	0	0
=2	3	4	2
=1	77	6	5
Totals =	97	14	7

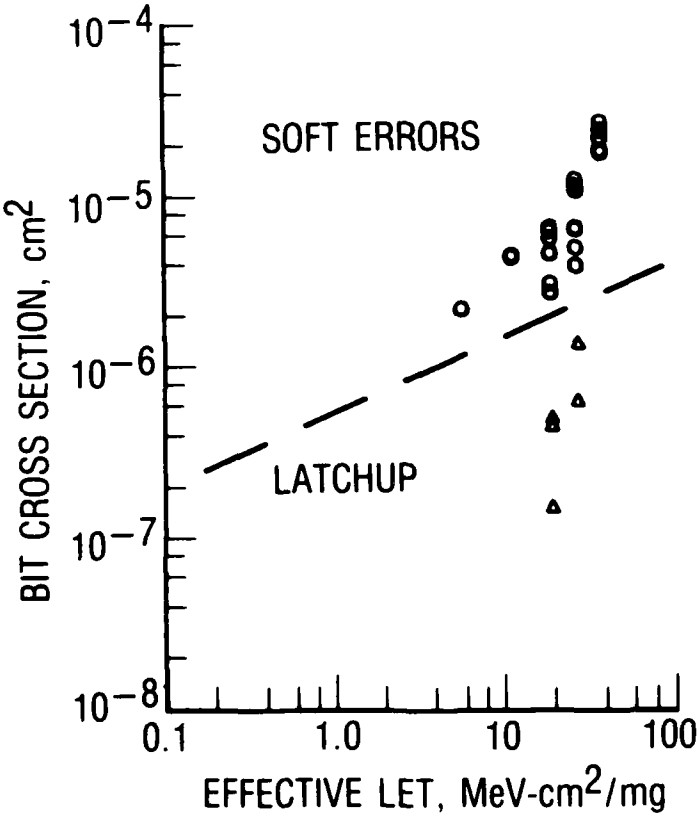


Fig. 7. Soft Upset and Latchup Cross Sections for the NSC 800. Latchup data includes "anomalous" rate error data. Soft error data includes random errors observed prior to the start of latchup (see text).

NSC-800 data are very incomplete, the gradual slope of the data and the lack of a discernable saturation in the cross section up to a LET of about 35 MeV-cm^2/mg lead to this speculation. An analysis similar to that given above for the Z-80 with more complete measurements could confirm this interpretation.

IV. CONCLUSIONS

The overall SEU cross section of a microprocessor can be resolved into cross sections for important sub-systems. The analysis presented above shows that the upset properties of the general purpose registers can be extracted from measured device data if sufficient attention is given to gathering complete data on each measured error.

Analysis of the heavy ion data for the Z-80 shows that all 208 general purpose register bits have the same upset threshold of 4.0 ± 0.5 MeV-cm^2/mg. Based upon measured data and photomicrographs we conclude that the Z-80 general purpose register bit has a saturation cross section of about $1.5 \times 10E\text{-}5$ cm^2.

The internal latches of the Z-80 play a dominant role in the upset of this device. The internal latches will upset for ions having LET as low as 0.7 MeV-cm^2/mg. Above the LET threshold for the general purpose registers, the internal latches contribute more errors than the general purpose registers.

The Z-80 heavy ion data show that the cosmic ray environment could upset certain internal latches in the Z-80 and cause contradictory signals to appear on the control bus. Among these control errors are: read/write active simultaneously; "halt" bit asserted; I/O and memory both active simultaneously; and the M1 bit toggled in the middle of an executing instruction. Depending on the system design, these unexpected signals may cause new kinds of system failures that need to be analyzed.

The Z-80 internal latches and general purpose registers are not sensitive to high energy protons in the 100 to 200 MeV range. Nuclear recoil upsets do occur at very high fluences.

The NSC-800 exhibits latchup and two varieties of non-random upset with greatly increased error rates over the random error rate. The corrected soft error cross section for the NSC-800 suggests that internal latches and not the general purpose registers are being upset below a LET of 35 MeV-cm^2/mg.

REFERENCES

1. C. S. Guenzer, A. B. Campbell, and P. Shapiro, "Single Event Upsets in NMOS Microprocessors," IEEE Trans. Nuc. Sci., NS-28, p. 3955-3957 (1981).

2. J. H. Adams, Jr., R. Silberberg, and C. H. Tsao, Cosmic Ray Effects on Microelectronics, Part I: The Near Earth Particle Environment, NRL Memorandum Report 4506 (August 25, 1981).

3. J. H. Adams Jr., J. R. Letlaw, and D. F. Smart, Cosmic Ray Effects on Microcircuits, Part II: The Geomagnetic Cutoff Effects, NRL Memorandum Report 5099 (May 26, 1983).

4. L. Edmonds, "Final Report: Cosmic Ray Environment Model for Earth Orbit," JPL Publication 84-98 (January 15, 1985).

5. J. H. Adams, Jr., "The Variability of Single Event Upset Rates in the Natural Environment," IEEE Trans. Nuc. Sci., NS-30, 4475-4480 (1983).

6. P. Shapiro, A. B. Campbell, E. L. Petersen, and L. T. Meyers, "Proton-Induced Single Event Upsets in NMOS Microprocessors," IEEE Trans. Nuc. Sci., NS-29, p. 2072-2074 (1982).

7. W. E. Will, K. A. Marks, and A. H. Johnston, "Total Dose Response of the Z80A and Z8002 Microprocessors," IEEE Trans. Nuc. Sci., NS-28, p. 4046-4050 (1981).

8. N. Wilkin, C. T. Self, and H. Eisen, "Ionizing Dose Rate Effects in Microprocessors," IEEE Trans. Nuc. Sci., NS-27, p. 1420-1424 (1980).

9. A. H. Johnston, "Annealing of Total Dose Damage in the Z80A Microprocessor," IEEE Nuc. Sci., NS-30, p. 4251-4255 (1983).

10. T. L. Criswell, P. R. Measel, and K. L. Wahlin, "Single Event Upset Testing with Relativistic Heavy Ions," IEEE Trans. Nuc. Sci. NS-31, p. 1559-1562 (1984).

11. R. Koga, and W. A. Kolasinski, "Heavy Ion-Induced Single Event Upsets of Microcircuits; A Summary of the Aerospace Corporation Test Data," IEEE Trans. Nuc. Sci. NS-31, p. 1190-1195 (1984).

12. S. E. Diehl-Nagel and J. E. Vinson, "Single Event Upset Rate Predictions for Complex Logic Systems," IEEE Trans. Nuc. Sci., NS-31, p. 1132-1138 (1984).

13. C. S. Guenzer, E. A. Wolicki, and R. [illegible]. Allas, "Single Event Upset of Dynamic Rams by Neutrons and Protons," IEEE Trans. Nuc. Sci., NS-26, p. 5048-5052 (1979).

14. E. L. Petersen, P. Shapiro, J. H. Adams, Jr., and E. A. Burke, "Calculation of Cosmic-Ray Induced Soft Upsets and Scaling in VLSI Devices," IEEE Trans. Nuc. Sci., NS-29, p. 2055-2063 (1982).

15. J. N. Bradford, "Microvolume Energy Deposition From High Energy Proton-Silicon Reactions," IEEE Trans. Nuc. Sci., NS-29, p. 2085-2089 (1982).

16. P. J. McNulty and G. E. Farrell, "Proton-Induced Nuclear Reactions in Silicon," IEEE Trans. Nuc. Sci., NS-28, p. 4007-4011 (1981).

17. D. K. Nichols and W. E. Price, "The Dependence of Single Event Upset on Proton Energy (15-590 MeV)," IEEE Trans. Nuc. Sci., NS-29, p. 2081-2084 (1982).

LABORATORY OPERATIONS

The Aerospace Corporation functions as an "architect-engineer" for national security projects, specializing in advanced military space systems. Providing research support, the corporation's Laboratory Operations conducts experimental and theoretical investigations that focus on the application of scientific and technical advances to such systems. Vital to the success of these investigations is the technical staff's wide-ranging expertise and its ability to stay current with new developments. This expertise is enhanced by a research program aimed at dealing with the many problems associated with rapidly evolving space systems. Contributing their capabilities to the research effort are these individual laboratories:

Aerophysics Laboratory: Launch vehicle and reentry fluid mechanics, heat transfer and flight dynamics; chemical and electric propulsion, propellant chemistry, chemical dynamics, environmental chemistry, trace detection; spacecraft structural mechanics, contamination, thermal and structural control; high temperature thermomechanics, gas kinetics and radiation; cw and pulsed chemical and excimer laser development including chemical kinetics, spectroscopy, optical resonators, beam control, atmospheric propagation, laser effects and countermeasures.

Chemistry and Physics Laboratory: Atmospheric chemical reactions, atmospheric optics, light scattering, state-specific chemical reactions and radiative signatures of missile plumes, sensor out-of-field-of-view rejection, applied laser spectroscopy, laser chemistry, laser optoelectronics, solar cell physics, battery electrochemistry, space vacuum and radiation effects on materials, lubrication and surface phenomena, thermionic emission, photosensitive materials and detectors, atomic frequency standards, and environmental chemistry.

Computer Science Laboratory: Program verification, program translation, performance-sensitive system design, distributed architectures for spaceborne computers, fault-tolerant computer systems, artificial intelligence, microelectronics applications, communication protocols, and computer security.

Electronics Research Laboratory: Microelectronics, solid-state device physics, compound semiconductors, radiation hardening; electro-optics, quantum electronics, solid-state lasers, optical propagation and communications; microwave semiconductor devices, microwave/millimeter wave measurements, diagnostics and radiometry, microwave/millimeter wave thermionic devices; atomic time and frequency standards; antennas, rf systems, electromagnetic propagation phenomena, space communication systems.

Materials Sciences Laboratory: Development of new materials: metals, alloys, ceramics, polymers and their composites, and new forms of carbon; nondestructive evaluation, component failure analysis and reliability; fracture mechanics and stress corrosion; analysis and evaluation of materials at cryogenic and elevated temperatures as well as in space and enemy-induced environments.

Space Sciences Laboratory: Magnetospheric, auroral and cosmic ray physics, wave-particle interactions, magnetospheric plasma waves; atmospheric and ionospheric physics, density and composition of the upper atmosphere, remote sensing using atmospheric radiation; solar physics, infrared astronomy, infrared signature analysis; effects of solar activity, magnetic storms and nuclear explosions on the earth's atmosphere, ionosphere and magnetosphere; effects of electromagnetic and particulate radiations on space systems; space instrumentation.

END

3-87

DTIC